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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,694	09/23/2003	Anthony Ciancio	SC12836ZP	2205

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,694	CIANCIO ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 8 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear to the examiner what a high dielectric constant material is when there is no indication of a reference point to determine what the level of high is meant to be.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-9, 11-12, 15-18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2004/0092073 Cabral, Jr. et al.

2. Referring to claim 1, a semiconductor device comprising: a semiconductor substrate, (Figure 29 #30 'Paragraph 0091 Lines 3-5'), a first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), formed over the semiconductor

substrate, (Figure 29 #30 'Paragraph 0091 Lines 3-5'); a first conductive smoothing layer, (Figure 29 #33 'Ta'), formed over the first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), wherein the first conductive smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"), has a surface roughness less than that of the first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"); a dielectric layer formed on the first conductive smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"); and a second electrode, (Figure 29 #81 'Paragraph 0097 Lines 3-4 'TiN" & 82 'Paragraph 0097 Lines 4-6 'Ti"), formed over the dielectric layer, (Figure 29 #34 Paragraph 0091 Lines 27-45).

3. Referring to claim 2, a semiconductor device, further comprising: a second conductive smoothing layer, (Figure 29 #35 'Paragraph 0091 Lines 46-49 'Ta"), formed between the dielectric layer, (Figure 29 #34 Paragraph 0091 Lines 27-45) and the second electrode, (Figure 29 #81 'Paragraph 0097 Lines 3-4 'TiN" & 82 'Paragraph 0097 Lines 4-6 'Ti"), wherein the second conductive smoothing layer, (Figure 29 #35 'Paragraph 0091 Lines 46-49 'Ta"), has a roughness less than that of the second electrode, (Figure 29 #81 'Paragraph 0097 Lines 3-4 'TiN" & 82 'Paragraph 0097 Lines 4-6 'Ti").

4. Referring to claim 3, a semiconductor device, wherein the second conductive smoothing layer comprises a refractory metal, (Figure 29 #35 'Paragraph 0091 Lines 46-49 'Ta").

5. Referring to claim 4, semiconductor device, wherein the first electrode comprises a first layer comprising a metal and a second layer comprising a refractory nitride, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), and the second

electrode comprises a metal, (Figure 29 #81 'Paragraph 0097 Lines 3-4 'TiN" & 82 'Paragraph 0097 Lines 4-6 'Ti").

6. Referring to claim 5, a semiconductor device, wherein the first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), and the second electrode comprise a refractory nitride, (Figure 29 #81 'Paragraph 0097 Lines 3-4 'TiN" & 82 'Paragraph 0097 Lines 4-6 'Ti").

7. Referring to claim 6, a semiconductor device, wherein the refractory nitride comprises a material selected from the group consisting of titanium nitride and tantalum nitride, (Figure 29 #32 'Paragraph 0091 Lines 14-19 'TaN" & #81 'Paragraph 0097 Lines 3-4 'TiN").

8. Referring to claim 8, a semiconductor device, wherein the dielectric layer comprises a high dielectric constant material, (Figure 29 #34 Paragraph 0091 Lines 27-45 and see the above 112 rejection).

9. Referring to claim 9, a semiconductor device, wherein the first electrode, the first conductive smoothing layer, the dielectric layer and the second electrode are part of a metal-insulator-metal (MIM) capacitor, (Figure 29).

10. Referring to claim 11, a semiconductor device comprising: a conductive layer, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), a smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"), formed in contact with the conductive layer, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), wherein the smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"), has a surface roughness less than that of the conductive layer, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"); and a dielectric layer, (Figure 29 #34

Paragraph 0091 Lines 27-45), formed in contact with the smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta").

11. Referring to claim 12, a semiconductor device, wherein the conductive layer comprises a metal, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN").

12. Referring to claim 15, a semiconductor device, wherein the conductive layer comprises a first layer comprising a metal and a second layer comprising a refractory nitride, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN").

13. Referring to 16, a semiconductor device, wherein the dielectric layer is a high dielectric constant material, (Figure 29 #34 Paragraph 0091 Lines 27-45 and see the above 112 rejection).

14. Referring to claim 17, a semiconductor device comprising: a semiconductor substrate, (Figure 29 #30 'Paragraph 0091 Lines 3-5'), a first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), formed over the semiconductor substrate, (Figure 29 #30 'Paragraph 0091 Lines 3-5'), wherein the first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), comprises a first layer comprising metal and a second layer over the first layer, wherein the second layer comprises a refractory nitride, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"); a first smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"), formed over the first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), wherein the first smoothing layer comprises a refractory metal, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"); a dielectric layer, (Figure 29 #34 Paragraph 0091 Lines 27-45), formed on the first smoothing layer, (Figure 29 #33

'Paragraph 0091 Lines 22-25 'Ta"); and a second electrode, (Figure 29 #81 'Paragraph 0097 Lines 3-4 'TiN" & 82 'Paragraph 0097 Lines 4-6 'Ti"), formed over the dielectric layer, (Figure 29 #34 Paragraph 0091 Lines 27-45), wherein the second electrode comprises a third layer comprising a refractory nitride and a fourth layer over the third layer, wherein the fourth layer comprises a metal, (Figure 29 #81 'Paragraph 0097 Lines 3-4 'TiN" & 82 'Paragraph 0097 Lines 4-6 'Ti").

15. Referring to claim 18, a semiconductor device, wherein the refractory nitride comprises a material selected from the group consisting of titanium nitride and tantalum nitride, (Figure 29 #32 'Paragraph 0091 Lines 14-19 'TaN" & #81 'Paragraph 0097 Lines 3-4 'TiN").

16. Referring to claim 20, a method for forming semiconductor device comprising: providing a semiconductor substrate, (Figure 29 #30 'Paragraph 0091 Lines 3-5'); forming a first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), formed over the semiconductor substrate, (Figure 29 #30 'Paragraph 0091 Lines 3-5'); forming a first conductive smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"), formed over the first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), wherein the first smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"), has a surface roughness less than that of the first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"); forming a dielectric layer, (Figure 29 #34 Paragraph 0091 Lines 27-45), formed on the first smoothing layer, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta"); and forming a second electrode, (Figure 29 #81 'Paragraph 0097 Lines 3-4 'TiN" & 82 'Paragraph 0097 Lines 4-6 'Ti"), formed over the dielectric layer, (Figure 29 #34 Paragraph 0091 Lines 27-45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 10, 13, 14, & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2004/0092073 Cabral, Jr. et al.

17. Referring to claim 7, a semiconductor device, wherein the first conductive smoothing layer comprises titanium, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta" and see * below).

* Cabral Jr. et al. discloses the claimed invention, but uses Ta for the smoothing layer or the like, Paragraph 0091 Lines 22-25 Figure 29 #33. It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Ti for Ta because both materials have very similar atomic size, weight, and electrical conductivity, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.
In re Leshin, 125 USPQ 416.

18. Referring to claim 10, a semiconductor device, further comprising: a capping layer over the first electrode, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN"), wherein the capping layer comprises a refractory nitride, (Figure 29 very top layer portion of #32 'Paragraph 0091 Lines 14-19 'TaN" and see ** below), and the first electrode comprises a metal, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN").

** It would be obvious to one having skill in the art at the time the invention was made to understand that the top portion of #32 is a layer that maybe a single atom layer and where the

portion of below that single atom layer is another layer, but thicker, thus it is obvious that a capping layer is on top of the first electrode and made out of a refractory nitride.

19. Referring to claim 13, a semiconductor device, wherein the conductive layer comprises titanium nitride, (Figure 29 #31 'Paragraph 0091 Lines 10-12 'Ti" & 32 'Paragraph 0091 Lines 14-19 'TaN" and see *** below), and the smoothing layer comprises titanium, (Figure 29 #33 'Paragraph 0091 Lines 22-25 'Ta" and see *** below).

*** */* Cabral Jr. et al. discloses the claimed invention, but uses Ta for the refractory material or the like, Paragraph 0091 Lines 22-25 Figure 29 #33. It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Ti for Ta because both materials have very similar atomic size, weight, and electrical conductivity, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.
In re Leshin, 125 USPQ 416.

20. Referring to claim 14, a semiconductor device, wherein the conductive layer, the smoothing layer and the dielectric layer are part of a device selected from the group consisting of a transistor and a capacitor, (Paragraphs 0018-0019).

It would be obvious to one having skill in the art at the time the invention was made to use the capacitor in a circuit, which contains transistors, (Paragraphs 0018-0019).

21. Referring to claim 19, a semiconductor device, wherein the refractory metal comprises titanium, (See */* below).

/ Cabral Jr. et al. discloses the claimed invention, but uses Ta for the refractory material or the like, Paragraph 0091 Lines 22-25. It would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute Ti for Ta because both materials have very similar atomic size, weight, and electrical conductivity, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.
In re Leshin, 125 USPQ 416.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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6/13/04